A1

and Associated Methods"; and U.S. Patent Application Serial No. 10/074,676, Attorney Docket No. SILA:098, titled "DC Offset Reduction in Radio-Frequency Apparatus and Associated Methods."

In the Claims:

Please cancel claim 2 and add new claims 3-78.

The rewritten clean versions of all the pending claims are provided below. Attached at the end of this paper is an Appendix providing an indication of the changes relative to the prior version of the claims, as now required by Rule 121(c).

A2

1. A receiver digital circuitry, comprising:

digital down-converter circuitry configured to mix a digital input signal provided by a receiver analog circuitry with an intermediate frequency (IF) local oscillator signal to generate a digital down-converted signal; and

digital filter circuitry configured to filter the digital down-converted signal to generate a filtered digital signal,

wherein the receiver analog circuitry resides within a first integrated circuit, and

wherein the receiver digital circuitry resides within a second integrated circuit, and the second integrated circuit couples to the first integrated circuit via a one-bit digital interface.

3. The receiver digital circuitry of claim 1, wherein the digital filter circuitry comprises a channelization filter circuitry.

4. The receiver digital circuitry of claim 3, wherein the digital input signal comprises a digital in-phase signal and a digital quadrature signal.

5. The receiver digital circuitry of claim 4, wherein the channelization filter circuitry comprises a cascade coupling of a cascade integrator/comb (CIC) filter circuitry and a secondary filter circuitry.

6. The receiver digital circuitry of claim 5, wherein the cascade integrator/comb filter circuitry comprises a cascade coupling of an integrator chain circuitry, a decimator circuitry, and a differentiator chain circuitry.

7. The receiver digital circuitry of claim 6, wherein the channelization filter circuitry provides a notch at minus a frequency of the intermediate frequency local oscillator signal.

8. The receiver digital circuitry of claim 7, wherein the secondary filter circuitry includes a cascade coupling of a notch circuitry and at least one biquad filter circuitry.

9. The receiver digital circuitry of claim 8, wherein the notch filter circuitry provides the notch at minus the frequency of the intermediate frequency local oscillator signal.

10. The receiver digital circuitry of claim 9, wherein the intermediate frequency local oscillator signal comprises a digital signal.

11. The receiver digital circuitry of claim 10, used within a radio-frequency transceiver circuitry.

12. The receiver digital circuitry of claim 10, further comprising a digital programmable gain amplifier circuitry configured to provide a programmable gain applied to the filtered digital signal to produce a digital scaled signal.

13. The receiver digital circuitry of claim 12, further comprising a digital-to-analog converter circuitry coupled to the digital programmable gain amplifier circuitry, the digital-to-analog converter circuitry configured to convert the digital scaled signal to an analog output signal.

14. The receiver digital circuitry of claim 13, wherein the digital-to-analog circuitry is further configured to provide the analog output signal to a baseband processor circuitry coupled to the receiver digital circuitry.

15. The receiver digital circuitry of claim 14 used within a radio-frequency transceiver circuitry.

16. A receiver digital circuitry, comprising:

digital filter circuitry configured to filter a digital input signal provided by a receiver analog circuitry to generate a filtered digital signal; and

digital down-converter circuitry configured to mix the filtered digital signal with an intermediate frequency (IF) local oscillator signal to generate a digital down-converted signal; and

wherein the receiver analog circuitry resides within a first integrated circuit, and

wherein the receiver digital circuitry resides within a second integrated circuit, and the second integrated circuit couples to the first integrated circuit via a one-bit digital interface.

17. The receiver digital circuitry of claim 16, wherein the digital filter circuitry comprises a channelization filter circuitry.

18. The receiver digital circuitry of claim 17, wherein the digital input signal comprises a digital in-phase signal and a digital quadrature signal.

19. The receiver digital circuitry of claim 18, wherein the channelization filter circuitry comprises a cascade coupling of a cascade integrator/comb (CIC) filter circuitry and a secondary filter circuitry.

20. The receiver digital circuitry of claim 19, wherein the cascade integrator/comb filter circuitry comprises a cascade coupling of an integrator chain circuitry, a decimator circuitry, and a differentiator chain circuitry.

21. The receiver digital circuitry of claim 20, wherein the channelization filter circuitry provides a notch at zero frequency.

22. The receiver digital circuitry of claim 21, wherein the secondary filter circuitry includes a cascade coupling of a notch circuitry and at least one biquad filter circuitry.

23. The receiver digital circuitry of claim 22, wherein the notch filter circuitry provides the notch at zero frequency.

24. The receiver digital circuitry of claim 23, wherein the intermediate frequency local oscillator signal comprises a digital signal.

25. The receiver digital circuitry of claim 24, used within a radio-frequency transceiver circuitry.

26. The receiver digital circuitry of claim 24, further comprising a digital programmable gain amplifier circuitry configured to provide a programmable gain applied to the digital down-converted signal to produce a digital scaled signal.

27. The receiver digital circuitry of claim 26, further comprising a digital-to-analog converter circuitry coupled to the digital programmable gain amplifier circuitry, the digital-to-analog converter circuitry configured to convert the digital scaled signal to an analog output signal.

28. The receiver digital circuitry of claim 27, wherein the digital-to-analog circuitry is further configured to provide the analog output signal to a baseband processor circuitry coupled to the receiver digital circuitry.

29. The receiver digital circuitry of claim 28, used within a radio-frequency transceiver circuitry.

30. The receiver digital circuitry of claim 24, further comprising a digital programmable gain amplifier coupled between the digital filter circuitry and the digital down-converter circuitry, the digital programmable gain amplifier circuitry configured to apply programmable gain to the digital filtered signal to produce a digital scaled signal, the digital programmable gain amplifier circuitry further configured to provide the digital scaled signal to the digital down-converter circuitry.

31. The receiver digital circuitry of claim 30, further comprising a digital-to-analog converter circuitry coupled to the digital down-converter circuitry, the digital-to-analog converter circuitry configured to convert the digital down-converted signal to an analog output signal.

32. The receiver digital circuitry of claim 31, wherein the digital-to-analog circuitry is further configured to provide the analog output signal to a baseband processor circuitry coupled to the receiver digital circuitry.

33. The receiver digital circuitry of claim 32, used within a radio-frequency transceiver circuitry.

34. A radio-frequency (RF) receiver circuitry, comprising:

a first integrated circuit, the first integrated circuit including receiver analog circuitry configured to receive and process a radio-frequency input signal to generate a processed radio-frequency signal, the receiver analog circuitry including an analog-to-digital converter circuitry adapted to convert the processed radio-frequency signal into a one-bit digital in-phase signal and a one-bit digital quadrature signal; and

a second integrated circuit, the second integrated circuit including receiver digital circuitry configured to receive the one-bit digital in-phase signal and the one-bit digital quadrature signal, the receiver digital circuitry further configured to process the one-bit digital in-phase signal and the one-bit digital quadrature signal to generate a baseband signal.

35. The radio-frequency receiver circuitry of claim 34, wherein the receiver digital circuitry further comprises digital down-converter circuitry configured to mix the one-bit digital one-phase signal and the one-bit digital quadrature signal to generate a digital down-converted in-phase signal and a digital down-converted quadrature signal.

36. The radio-frequency receiver circuitry of claim 35, wherein the receiver digital circuitry further comprises a digital channelization filter circuitry coupled to the digital down-converter circuitry, and wherein the digital channelization filter circuitry receives the digital down-converted in-phase signal and the digital down-converted quadrature signal.

37. The radio-frequency receiver circuitry of claim 36, wherein the digital channelization filter filters the digital down-converted in-phase signal and the digital down-converted quadrature signal to generate, respectively, a digital filtered in-phase signal and a digital filtered quadrature signal.

38. The radio-frequency receiver circuitry of claim 37, wherein the channelization filter further comprises a cascade coupling of a digital cascade integrator/comb filter circuitry and a digital filtering circuitry.

39. The radio-frequency receiver circuitry of claim 38, wherein the cascade integrator/comb filter circuitry comprises a cascade coupling of an integrator chain circuitry, a decimator circuitry, and a differentiator chain circuitry.

40. The radio-frequency receiver circuitry of claim 39, wherein the channelization filter circuitry provides a notch at minus a frequency of the intermediate frequency local oscillator signal.

41. The radio-frequency receiver circuitry of claim 40, wherein the digital filtering circuitry includes a cascade coupling of a notch filter circuitry and at least one biquad filter circuitry.

42. The radio-frequency receiver circuitry of claim 41, wherein the notch filter circuitry provides the notch at minus the frequency of the intermediate frequency local oscillator signal.

43. The radio-frequency receiver circuitry of claim 42, wherein the intermediate frequency local oscillator signal comprises a digital signal.

44. The radio-frequency receiver circuitry of claim 43, wherein the receiver digital circuitry further comprises a digital programmable gain amplifier circuitry configured to apply a first programmable gain to the digital filtered in-phase signal to produce a scaled digital in-phase signal, the digital programmable gain amplifier circuitry further configured to apply a second programmable gain to the digital filtered quadrature signal to produce a scaled digital quadrature signal.

45. The radio-frequency receiver circuitry of claim 44, wherein the receiver digital circuitry further comprises a digital-to-analog converter circuitry coupled to the digital programmable gain amplifier circuitry, the digital digital-to-analog circuitry configured to convert the scaled digital in-phase signal to an analog in-phase signal, the digital-to-analog circuitry further configured to convert the scaled digital quadrature signal to an analog quadrature signal.

46. The radio-frequency receiver circuitry of claim 45, wherein the digital-to-analog circuitry is further configured to provide the analog in-phase signal and the analog quadrature signal to a baseband processor circuitry coupled to the receiver digital circuitry.

47. The radio-frequency receiver circuitry of claim 46 used within a radio-frequency transceiver circuitry.

48. The radio-frequency receiver circuitry of claim 34, wherein the receiver digital circuitry further comprises a digital channelization filter circuitry configured to receive the one-bit digital in-phase signal and the one-bit digital quadrature signal.

49. The radio-frequency receiver circuitry of claim 48, wherein the digital channelization filter filters the one-bit digital in-phase signal and the one-bit digital

quadrature signal to generate, respectively, a digital filtered in-phase signal and a digital filtered quadrature signal.

50. The radio-frequency receiver circuitry of claim 49, wherein the receiver digital circuitry further comprises digital down-converter circuitry coupled to the digital channelization filter circuitry, the digital down-converter circuitry configured to mix the digital filtered in-phase signal and the digital filtered quadrature signal with an intermediate frequency local oscillator signal to generate a digital down-converted in-phase signal and a digital down-converted quadrature signal.

51. The radio-frequency receiver circuitry of claim 50, wherein the channelization filter further comprises a cascade coupling of a digital cascade integrator/comb filter circuitry and a digital filtering circuitry.

52. The radio-frequency receiver circuitry of claim 51, wherein the cascade integrator/comb filter circuitry comprises a cascade coupling of an integrator chain circuitry, a decimator circuitry, and a differentiator chain circuitry.

53. The radio-frequency receiver circuitry of claim 52, wherein the channelization filter circuitry provides a notch at zero frequency.

54. The radio-frequency receiver circuitry of claim 53, wherein the digital filtering circuitry includes a cascade coupling of a notch filter circuitry and at least one biquad filter circuitry.

55. The radio-frequency receiver circuitry of claim 54, wherein the notch filter circuitry provides the notch at zero frequency.

56. The radio-frequency receiver circuitry of claim 55, wherein the intermediate frequency local oscillator signal comprises a digital signal.

57. The radio-frequency receiver circuitry of claim 56, wherein the receiver digital circuitry further comprises a digital programmable gain amplifier circuitry configured to apply a first programmable gain to the digital down-converted in-phase signal to generate a scaled in-phase digital down-converted signal, the programmable gain amplifier circuitry configured to apply a second programmable gain to the digital down-converted quadrature signal to generate a scaled quadrature digital down-converted signal.

58. The radio-frequency receiver circuitry of claim 57, wherein the receiver digital circuitry further comprises a digital-to-analog converter circuitry coupled to the digital programmable gain amplifier circuitry, the digital digital-to-analog circuitry configured to convert the scaled in-phase digital down-converted signal to an analog in-phase signal, the digital-to-analog converter circuitry further configured to convert the scaled quadrature digital down-converted signal to an analog quadrature signal.

59. The radio-frequency receiver circuitry of claim 58, wherein the digital-to-analog circuitry is further configured to provide the analog in-phase signal and the analog quadrature signal to a baseband processor circuitry coupled to the receiver digital circuitry.

60. The radio-frequency receiver circuitry of claim 59, used within a radio-frequency transceiver circuitry.

61. A method of receiving a radio-frequency (RF) signal, comprising:

receiving and processing the radio-frequency signal within a first integrated circuit that includes receiver analog circuitry configured to generate an analog processed radio-frequency signal;

converting the analog processed radio-frequency signal within the first integrated circuit to a digital signal;

supplying the digital signal via a one-bit digital interface;

receiving the digital signal within a second integrated circuit that includes receiver digital circuitry;

mixing within the digital receiver circuitry the digital signal with a digital intermediate frequency (IF) local oscillator signal to generate a digital down-converted signal; and

processing the digital down-converted signal within the receiver digital circuitry to generate a baseband signal.

62. The method of claim 61, wherein processing the digital down-converted signal further comprises performing digital channelization filtering of the digital down-converted signal to generate a filtered digital signal.

63. The method of claim 62, wherein performing digital channelization filtering of the digital down-converted signal further comprises filtering the digital down-converted signal with a cascade integrator/comb filter circuitry to generate an output signal of the cascade integrator/comb filter circuitry.

64. The method of claim 63, wherein performing digital channelization filtering of the digital down-converted signal further comprises filtering the output signal of the cascade integrator/comb filter circuitry to generate a filtered output signal.

65. The method of claim 64, wherein performing digital channelization filtering further comprises inserting a notch in the filtered output signal at minus a frequency of the intermediate frequency local oscillator signal to generate a notched digital signal.

66. The method of claim 65, further comprising applying a digital programmable gain to the notched digital signal to produce a scaled digital signal.

67. The method of claim 66, further comprising converting the scaled digital signal to an analog signal.

68. The method of claim 67, further comprising supplying the analog signal to a baseband processor circuitry.

69. The method of claim 68, further comprising receiving the radio-frequency signal within a radio-frequency transceiver circuitry.

70. A method of receiving a radio-frequency (RF) signal, comprising:

receiving and processing the radio-frequency signal within a first integrated circuit that includes receiver analog circuitry configured to generate an analog processed radio-frequency signal;

converting the analog processed radio-frequency signal within the first integrated circuit to a digital signal;

supplying the digital signal via a one-bit digital interface;

receiving the digital signal within a second integrated circuit that includes receiver digital circuitry;

performing digital channelization filtering of the digital signal within the receiver digital circuitry to generate a filtered digital signal; and

processing the filtered digital signal within the receiver digital circuitry to generate a baseband signal.

71. The method of claim 70, wherein processing the filtered digital signal further comprises mixing the filtered digital signal with a digital intermediate frequency local oscillator signal to generate a digital down-converted signal.

72. The method of claim 71, wherein performing digital channelization filtering of the digital signal further comprises filtering the digital signal with a cascade integrator/comb filter circuitry to generate a filtered output signal of the cascade integrator/comb filter circuitry.

73. The method of claim 72, wherein performing digital channelization filtering of the digital signal further comprises filtering the output signal of the cascade integrator/comb filter circuitry to generate a filtered output signal.

74. The method of claim 73, wherein performing digital channelization filtering further comprises inserting a notch in the filtered output signal at zero frequency.

75. The method of claim 74, further comprising applying a digital programmable gain to the digital down-converted signal to produce a scaled digital signal.

76. The method of claim 75, further comprising converting the scaled digital signal to an analog signal.

77. The method of claim 76, further comprising supplying the analog signal to a baseband processor circuitry.

78. The method of claim 77, further comprising receiving the radio-frequency signal within a radio-frequency transceiver circuitry.

CONCLUSION

With this amendment, claims 1 and 3-78 are pending. Claim 2 has been cancelled. A check in the amount of $1,194.00 is enclosed for the addition of 57 dependent claims and 2 independent claims.

Should any fees under 37 CFR 1.16-1.21 be required for any reason relating to the enclosed materials, the Commissioner is authorized to deduct such fees from Deposit Account No. 10-1205/SILA:078. The examiner is invited to contact the undersigned at the phone number indicated below with any questions or comments, or to otherwise facilitate expeditious and compact prosecution of the application.

Respectfully submitted,

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